Our innovative and growing company is searching for experienced candidates for the position of pre-silicon validation engineer. If you are looking for an exciting place to work, please take a look at the list of qualifications below.

Responsibilities for pre-silicon validation engineer

- When appropriate, verify low power design features at the subsystem level using power-aware verification technique and formal verification
- Plan and implement the UVM testbench, functional coverage model and assertions
- Close collaboration with architects and logic/analog designers
- Validation of an IP or feature, either directly or at the system level
- Creating plans and tests for validating portions of a complex microarchitecture using written specs, RTL code and other tests as a guide
- Learning the architecture and microarchitecture by debugging failures to the root cause
- Developing and utilizing various debug and validation tools and/or methodologies to implement validation plans with the goal being to ensure a solid design
- Participating in the debug of failures on silicon and developing new testing strategies to detect these failures on RTL models
- Engaging with IP providers and customers to define, develop and deliver necessary infrastructure and address issues found during execution
- Developing tools and methods to streamline IP development and SOC integration to deliver highest quality in shortest time possible

Qualifications for pre-silicon validation engineer

- Set aggressive goals and meet the commitments
- SOC microarchitecture and system level skills
- Chip and/or system / platform level Validation / Verification
- Knowledge in IA architecture / Multiple Operating Systems / SW / FW /