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# Example of Design Eng Job Description

Our company is growing rapidly and is looking to fill the role of design eng. Please review the list of responsibilities and qualifications. While this is our ideal list, we will consider candidates that do not necessarily have all of the qualifications, but have sufficient experience and talent.

## Responsibilities for design eng

* Use/enhance performance and power models to project performance per watt of future products and evaluate power impact of proposed design changes
* Liaise software and hardware design teams to quantify implementation costs for new features, and consideration of other techniques to save power or improve performance per watt
* Review designs and track progress/improvement
* Lead the development of power model that can work in concert with architectural performance models to predict performance per watt
* Coordinate diagnostics’ development to enable model correlation studies, competitive analysis and identification of improvement opportunities
* Develop strategies to enhance model to reflect [new] power management policies that may be implemented in software, firmware and/or hardware
* Work with verification and hardware emulation teams to leverage power model for automated power regression testing and analysis
* Work on leading edge wireless technologies/standards such as 802.11ax WLAN & BT/BLE5
* Be responsible for complete application hardware development from design concept to production including tuning RF front end components and calibrations
* Interact with silicon designers & software/firmware teams to realize highest performance, industry leading solutions in the Enterprise and Service Provider markets

## Qualifications for design eng

* Configuration Management (CM) comprehension and aptitude to develop advanced TDP record set management techniques in a Product Data Management System (PDM)
* IP/MPLS Certification
* Experience with engineering design software will be an advantage
* FPGA design experience with tools noted above
* Should have good experience leading chip level implementation from Netlist to GDSII physical design implementation flow at block level (2M plus) top level, including floorplanning, placement, signal & clock routing, static timing analysis, power analysis and Physical Verification & extraction using industry standard tools
* Candidate should be knowledgeable in PERL/TCL/AWK/Shell scripting