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# Example of ASIC / Layout Design Engineer Job Description

Our company is searching for experienced candidates for the position of ASIC / layout design engineer. To join our growing team, please review the list of responsibilities and qualifications.

## Responsibilities for ASIC / layout design engineer

* Leading a small group of engineers to conquer challenging verification work
* Write tests in C, C++ and located bugs in simulation
* Work closely with architects and designers
* Co-coordinating across team in SoC or other IP during daily work
* Work in close collaboration with the front end designers and architects on the various SOC performace verification efforts
* Work with architects, and the design and DV team to develop functional and perfrormance Testplan
* Collaborate with analog designers to understand the circuit that the RTL is interacting with
* Analysis and debug of test failures
* The successful candidate will report to the SOC DFT (Design-For-Test) DV Manager and will have the following responsibilities
* Work with global Front-End design team and architect team for functional or performance verification verification for Graphics Chip

## Qualifications for ASIC / layout design engineer

* For new college grads (less than 2 years experience), minimum GPA of 3.5 required for consideration
* Experience with perl or similar scripting languages
* Passion for ASIC validation
* BS (or MS) in EE, CS, CSE plus 2+ (or 0 with MS) years ASIC hardware design/verification experience
* Experience with Verilog, System Verilog required
* Experience with C/C++, SVA/PSL, and Perl a plus