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# Example of ASIC Digital Design Engr Job Description

Our innovative and growing company is looking for an ASIC digital design engr. If you are looking for an exciting place to work, please take a look at the list of qualifications below.

## Responsibilities for ASIC digital design engr

* Participate in the discussions and reviews of DFT to improve the correctness and efficiency of the DFT flow
* Study standard specifications published by JEDEC
* Define micro architecture at block level based on IP architecture
* Work on RTL design based on predefined coding style, SVA is also included
* Clean RTL check violations in lint, CDC, DFT and synthesis
* Run block level test to speed up IP verification
* Work with verification to debug and fix RTL issues
* Check synthesis timing and improve RTL design if required
* This is a position in leading edge IP Verification
* Develop and execute verification for IP level features related to Interface IP system

## Qualifications for ASIC digital design engr

* Must have hands-on experience in writing complex testcases in Verilog and System Verilog
* Must have familiarity with code quality metrics
* Must have deep understanding of asynchronous clock crossings, DFT design methodologies, and synthesis implications of RTL
* Verification IP Development/Verification of IP Cores or SoC Designs for Set Top Boxes, Mobile handsets, Smart Devices
* Hands on experience in Verification IP or certain components of Test Environment coding, test case development and debug
* Bachelor’s degree in engineering is required with minimum 2 years of relevant experience in RTL functional verification